Homework 1 – PN- Junction and MOSFET

PN- Junction

Problem 1

Consider a silicon PN step junction diode with Nd = $10^{16}cm^{-3}$ and Na = 5 x$10^{15}cm^{-3}$. Assume T = 300 K.

(a) Calculate the built-in potential ψ_{bi}

(b) Calculate the depletion-layer width (W_{dep}) and its length on the N side (x_n) and P side (x_p).

(c) Calculate the maximum electric field.

(d) Sketch the energy band diagram, electric potential, electric field distribution, and the space-charge profile.

(e) Now let Na = $10^{18}cm^{-3}$. Repeat (a), (b), and (c). Compare these to the previous results. How have the depletion widths changed, And built-in voltage?

Problem 2: Narrow-Base Diode

Consider an ideal pn^+ step-junction Si diode maintained at 300K with cross-sectional area A = 10^{-4} cm^2. The doping concentration on the p-type side is $N_A = 10^{17}$ cm^{-3} . (The n-type side is degenerately doped.) The electron recombination lifetime in the p-type region is $\tau_n = 10^{-6}$ s. The width of the quasi-neutral p-type region is 1 μm, for V_A = 0 V.

a) Is this a narrow-base diode? Justify your answer.

b) Calculate the diode saturation current I_0.

c) What value of applied bias V_A is required to obtain a diode current of 1 mA?

How would your answer to part **(c)** change if the width of the p-type region is reduced? Explain briefly

MOSFET

Problem 1

The relationship between the charge in the inversion layer and the gate voltage is as follows:
$Qn=C_i(V_G-V_T)$

a) Draw band diagrams of an ideal p type substrate MOS capacitor under $V_G=V_T$ and $V_G>V_T$ including the oxide layer and metal gate.
b) Draw a schematic diagram of the charge distribution in these two cases.
c) Explain qualitatively why the relationship above holds
d) Derive mathematically the relationship above. (what is the relationship between the field in the oxide layer, the edge of the silicon layer and the inversion layer charge? How does this field relate to the gate voltage?(use the delta-depletion approximation)

Problem 2

Consider an ideal MOS capacitor fabricated on a P-type silicon with a doping level of $N_A = 5 \times 10^{16}$ cm^{-3} with an oxide thickness of 2 nm and an N^+ poly-gate .

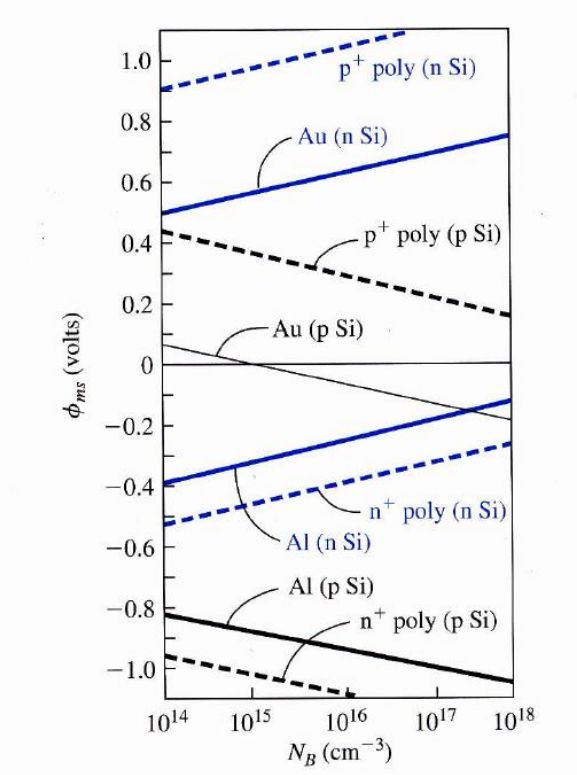


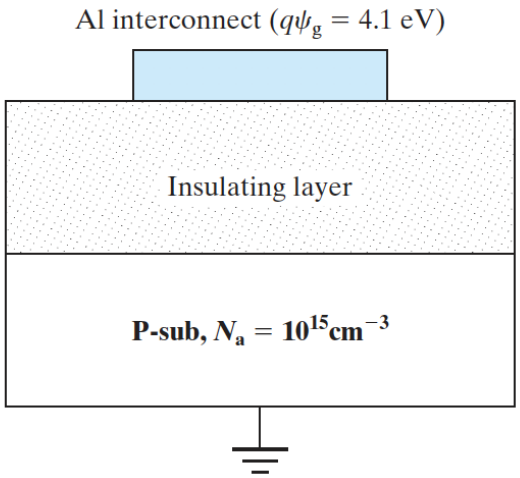
Figure 1. Metal-semiconductor work function difference versus doping for aluminum, gold. and n+ and p+ polysilicon gates.

(a) What is the flat-band voltage, V_{fb}, of this capacitor?
(b) Calculate the maximum depletion region width, W_{dmax}.

(c) Find the threshold voltage, V_t, of this device.
(d) If the gate is changed to P^+ poly, what would the threshold voltage be now?

Problem 3

Metal interconnect lines in integrated circuits (ICs) form parasitic MOS capacitors as illustrated in the following figure. Generally, one wants to prevent the underlying Si substrate from becoming inverted. Otherwise, parasitic transistors may be formed and create undesirable current paths between the N^+ diffusions.



(a) Find V_{fb} of this parasitic MOS capacitor.
(b) If the interconnect voltage can be as high as 5 V, what is the maximum capacitance (F/cm^2) of the insulating layer that can be tolerated without forming an inversion layer?
(c) If the insulating layer thickness must be 1 μm for fabrication considerations, what should the dielectric constant $\varepsilon_s = \varepsilon_r \cdot \varepsilon_0$ where ε_r is the dielectric constant of the insulator and ε_0 is the dielectric constant of the vacuum. of the insulating material be to make V_t = 5V?
(d) Is the answer in (c) the minimum or maximum allowable ε_r to prevent inversion?
(e) At $V_g = V_t + 2$ V (V_t = 5 V), what is the area charge density (C/cm^2) in the inversion layer?
(f) At $V_g = V_t + 2$ V (V_t = 5 V), what voltage is dropped across the insulating layer?